by driving the emitter/sourceline **407** negative and by driving the write data word line **432**, connected to the base/source region **411-1**, positive to achieve a coincident address at one location. This is illustrated in more detail in the schematic embodiment shown in FIG. **4**D. The cell, **401-1**, can be erased by driving the drain **415-1** positive and by driving the gate **419-1** negative to forward bias the drain-body p-n junction.

FIG. **4**C illustrates an embodiment for another mode of operation for a vertical merged MOS-bipolar-capacitor memory gain cell, e.g. **401-1**, according to the teachings of the present invention. In the mode of operation, shown in FIG. **4**C, the embodiment allows provisions for biasing a body capacitor plate line **431** to a positive potential. In this embodiment, biasing a body capacitor plate line **431** can be used in conjunction with a positive read data word line **419-1** voltage to drive the n-type body **413-1** and the p-type source and drain, **411-1** and **415-1** respectively, junctions to a larger reverse bias during standby. This insures that the floating body **413-1** will not become forward biased during standby. Thus, stored charge will not be lost due to leakage currents with forward bias.

FIG. **5** is a block diagram of a processor-based system **500** utilizing a vertical merged MOS-bipolar-capacitor memory gain cell according to the various embodiments of the present invention. That is, the system **500** utilizes various embodiments of the memory cell illustrated in FIGS. **4**A–**4**D. The processor-based system **500** may be a computer system, a process control system or any other system employing a processor and associated memory. The system **500** includes a central processing unit (CPU) **502**, e.g., a microprocessor, that communicates with the RAM **512** and an I/O device **508** over a bus **520**. It must be noted that the bus **520** may be a series of buses and bridges commonly used in a processor-based system, but for convenience purposes only, the bus **520** has been illustrated as a single bus. A second I/O device **510** is illustrated, but is not necessary to practice the invention. The processor-based system **500** also includes read-only memory (ROM) **514** and may include peripheral devices such as a floppy disk drive **504** and a compact disk (CD) ROM drive **506** that also communicates with the CPU **502** over the bus **520** as is well known in the art.

It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device **500** has been simplified to help focus on the invention.

It will be understood that the embodiment shown in FIG. **5** illustrates an embodiment for electronic system circuitry in which the novel memory cells of the present invention are used. The illustration of system **500**, as shown in FIG. **5**, is intended to provide a general understanding of one application for the structure and circuitry of the present invention, and is not intended to serve as a complete description of all the elements and features of an electronic system using the novel memory cell structures. Further, the invention is equally applicable to any size and type of system **500** using the novel memory cells of the present invention and is not intended to be limited to that described above. As one of ordinary skill in the art will understand, such an electronic system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.

Applications containing the novel memory cell of the present invention as described in this disclosure include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others.

METHODS OF FABRICATION

The inventor has previously disclosed a variety of vertical devices and applications employing transistors along the sides of rows or fins etched into bulk silicon or silicon on insulator wafers for devices in array type applications in memories. (See generally, U.S. Pat. Nos. 6,072,209; 6,150,687; 5,936,274 and 6,143,636; 5,973,356 and 6,238,976; 5,991,225 and 6,153,468; 6,124,729; 6,097,065). The present invention uses similar techniques to fabricate the single transistor vertical memory gain cell described herein. Each of the above referenced US Patents is incorporated in full herein by reference.

FIG. **6**A outlines one embodiment of a fabrication technique for merged MOS-bipolar-capacitor memory gain cells where the emitter/sourceline **602** are separated and can be biased. In the embodiment of FIG. **6**A, a p-type substrate **601** has been processed to include layers thereon of an n+ conductivity type **602**, a p conductivity type **603**, an n conductivity type **604**, and a p+ conductivity type **605**. In the embodiment of FIG. **6**A, the fabrication continues with the wafer being oxidized and then a silicon nitride layer (not shown) is deposited to act as an etch mask for an anisotropic or directional silicon etch which will follow. This nitride mask and underlying oxide are patterned and trenches are etched as shown in both directions, leaving blocks of silicon, e.g. **600-1**, **600-2**, **600-3**, and **600-4**, having alternating layers of n and p type conductivity material. Any number of such blocks can be formed on the wafer. In the embodiment of FIG. **6**A, two masking steps are used and one set of trenches, e.g. trench **610**, is made deeper than the other, e.g. trench **609**, in order to provide separation and isolation of the emitter/source lines **602**.

FIG. **6**B illustrates a perspective view taken at cut line **6**B—**6**B from FIG. **6**A. In FIG. **6**B, both trenches **609** and **610** are filled with oxide **607** and the whole structure is planarized such as by CMP. As shown in FIG. **6**B, the oxide **615** in the write data word line blocks, trench **610**, are recessed to near the bottom and just above the bottom of the p-type regions **603** in the pillars, **600-1**, **600-2**, **600-3**, and **600-4**. In the embodiment shown in FIG. **6**B, p-type polysilicon **615** is deposited and planarized to be level with the tops of the pillars and then recessed to just below the top of the p-type regions **603** in the pillars, **600-1**, **600-2**, **600-3**, and **600-4**. This p-type poly **615** and the p-type regions **603** in the pillars **600-1**, **600-2**, **600-3**, and **600-4** will form the write data word lines, shown as **432** in FIGS. **4**B and **4**C.

In FIG. **6**C, oxide is again deposited and then planarized to the top of the pillars. Next, the trenches **609** for the read data word lines, shown as **421-1** in FIGS. **4**B and **4**C, and the capacitor plate lines, shown as **431** in FIG. **4**C, are opened.

FIG. **6**D illustrates a cross-sectional view taken along cut line **6**D—**6**D in FIG. **6**C. This remaining structure, as shown in the embodiment of FIG. **6**D, can then be continued by conventional techniques including gate oxidation and deposition and anisotropic etch of polysilicon along the sidewalls to form body capacitor plate, e.g. **405-1** in FIGS. **4**A–**4**C, and read data word lines, e.g. **421-1** in FIGS. **4**B and **4**C. The